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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/055,722	01/23/2002	Akio Kitamura	FUJI:203	6219

7590 11/20/2002
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P.O. Box 826
Ashburn, VA 20146-0826

EXAMINER

FENTY, JESSE A

ART UNIT	PAPER NUMBER
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2815

DATE MAILED: 11/20/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/055,722

Applicant(s)

KITAMURA, AKIO

Examiner

Jesse A. Fenty

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 01 November 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) 9 and 10 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-8 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 5.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election of Group I, claims 1-8 in Paper No. 8 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

2. Claims 9 and 10 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim.

Election was made **without** traverse in Paper No. 8.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

4. Claims 1-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Williams et al. (U.S. Patent No. 5,541,125).

In re claim 1, Williams discloses a semiconductor device, comprising:

A semiconductor substrate (10);

A first MOS transistor (16V NMOS) and a second MOS transistor (20V NMOS) integrated in the semiconductor substrate, wherein said second MOS transistor has a lower threshold voltage than said first MOS transistor and said first MOS transistor has a smaller channel length than said second MOS transistor; and

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A punch-through stopper area (P-Well) that surrounds a source area and a drain are of said first MOS transistor and provides a punch-through voltage resistance between said source area and said drain area.

In re claim 2, Williams discloses the device of claim 1. The distinction between the first and second MOS transistors composing digital and analog devices respectively are recitations of the intended use of the claimed device. Terms that simply set forth the intended use, a property inherent in or a function, do not differentiate the claimed composition of these elements from those known to prior art.

In re claim 3, Williams discloses the device of claim 1, wherein a drain area (152) of said second MOS transistor is surrounded by an offset drain area (122) having a lower impurity concentration than the drain are of the second MOS transistor.

In re claim 4, Williams discloses the device of claim 3, further comprising a punch-through stopper area (corresponding 122) that surrounds a source area (corresponding 152) of said second MOS transistor and provides a punch-through voltage resistance between the source area of said second MOS transistor and said offset drain area.

In re claim 5, Williams discloses the device of claim 1, further comprising a bipolar transistor integrated in said semiconductor substrate.

In re claim 6, Williams discloses the device of claim 1, further comprising a diode (there are many PN junction-diodes in the device) integrated in said semiconductor substrate.

In re claim 7, Williams discloses the device of claim 1, further comprising a diffusion resistor integrated in said semiconductor substrate.

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In re claim 8, Williams discloses the device of claim 1, wherein said source area includes a source LDD area and said drain area includes a drain side LDD area, and wherein the punch-through stopper area (P-well) has a pocket structure and at encloses the source side LDD area and the drain side LDD area.

Conclusion

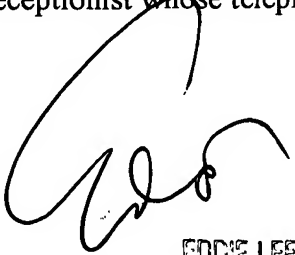
5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Krivokapic et al. (U.S. Patent No. 6,238,982 B) and Kumagai (U.S. Patent No. 6,329,693 B1) disclose similar inventions to the instant application.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse A. Fenty whose telephone number is 703-308-8137. The examiner can normally be reached on 5/4-9 1st Fri. Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 703-308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-746-3892 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

JAF
November 18, 2002


EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2300

Jesse A. Fenty
Examiner
Art Unit 2815